REMARKS

The Office Action dated October 5, 2009 was received and carefully reviewed.

Claims 1-27 and 29-47 were pending in the subject application, prior to this response. Presently, claims 18, 31, and 32 are hereby amended to clarify the invention, and not for reasons of patentability. New claims 48 and 49 have been added by way of this response. Accordingly, claims 1-27 and 29-49 are currently pending in the subject application.

Support for the subject matter seen in new claims 48 and 49 can be found, e.g., in FIG. 5 and page 33, line 20 through page 34, line 10 of the specification as originally filed. Thus, Applicants contend that newly added claims 48 and 49 do not include new matter.

Reconsideration and withdrawal of all currently pending rejections is hereby requested in view of the comments advanced in detail below.

Allowable Subject Matter

Applicants acknowledge the allowance of claims 1-17, 19-27, 29, 30, 36, 37, and 39-47.

Claim Rejections - 35 U.S.C. § 103

Claims 18, 31-35, and 38 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Hashimoto et al. (U.S. Pat. Pub. No. 2003/0083203 A1) (*Hashimoto*, hereinafter) in view of Kimura et al. (U.S. Pat. Pub. No. 2004/0142544 A1) (*Kimura*, hereinafter). Applicants traverse this rejection for at least the reasons set forth below.

Applicants respectfully submit that present independent claims 18, 31, and 32, and the claims dependent therefrom, are patently distinguishable over *Hashimoto* and *Kimura*, taken either alone or in combination, since *Hashimoto* and *Kimura* fail to disclose, teach, or suggest all of the features recited in the pending claims. For example, independent claim 18 (emphasis added) recites:

> 18. A method for manufacturing a thin film transistor, comprising the steps of:
>
> forming a source electrode and a drain electrode;
>
> forming a semiconductor film over the source electrode and the drain electrode and between the source electrode and the

drain electrode;

forming a gate insulating film to cover the semiconductor film;

forming a first liquid-repellent region by a plasma treatment on a surface for forming a gate electrode in an upper portion of the gate insulating film;

forming selectively a first lyophilic region in the first liquid-repellent region; and

forming the gate electrode in the first lyophilic region of the surface of the semiconductor film by dropping a composition including a first conductive material.

Further, independent claim 31 (emphasis added) recites:

31. A droplet discharging method, comprising the steps of:

forming selectively a lyophilic region by irradiating selectively an object to be treated in which a liquid-repellent region is formed with light by a light irradiation unit so that the object to be treated includes the lyophilic region and the liquid-repellent region; and

discharging a droplet onto the lyophilic region by a droplet discharging unit, in a treatment chamber including the droplet discharging unit and the light irradiation unit.

Furthermore, independent claim 32 (emphasis added) recites:

32. A droplet discharging method, using a treatment apparatus in which a first treatment chamber having a plasma unit and a dielectric, and a second treatment chamber having a droplet discharging unit and a light irradiation unit, comprising the steps of:

forming a liquid-repellent region in an object to be treated by the plasma unit and the dielectric in the first treatment chamber;

transporting the object to be treated into the second treatment chamber without being exposed to the atmosphere;

forming selectively a lyophilic region by irradiating

selectively the object to be treated in which the liquid-repellent region is formed with light by the light irradiation unit in the second treatment chamber so that the object to be treated includes the lyophilic region and the liquid-repellent region; and

discharging a droplet onto the lyophilic region by the droplet discharging unit.

As seen above, independent claim 18 is directed to, *inter alia*, a method of manufacturing a thin film transistor including at least the feature of forming selectively a first lyophilic region in the first liquid-repellent region. As also seen above, independent claim 31 is directed to, *inter alia*, a droplet discharging method including at least the feature of forming selectively a lyophilic region by irradiating selectively an object to be treated in which a liquid-repellent region is formed with light by a light irradiation unit so that the object to be treated includes the lyophilic region and the liquid-repellent region. Additionally, independent claim 32 is directed to, *inter alia*, a droplet discharging method including at least the feature of forming selectively a lyophilic region by irradiating selectively the object to be treated in which the liquid-repellent region is formed with light by the light irradiation unit in the second treatment chamber so that the object to be treated includes the lyophilic region and the liquid-repellent region.

Applicants contend that *Hashimoto* and *Kimura*, taken either alone or in combination, fail to disclose, teach or suggest a method of manufacturing a thin film transistor including at least the feature of forming selectively a first lyophilic region in the first liquid-repellent region, as recited in present independent claim 18. Applicants also contend that *Hashimoto* and *Kimura*, taken either alone or in combination, fail to disclose, teach or suggest a droplet discharging method including at least the feature of forming selectively a lyophilic region by irradiating selectively an object to be treated in which a liquid-repellent region is formed with light by a light irradiation unit so that the object to be treated includes the lyophilic region and the liquid-repellent region, as recited in present independent claim 31. In addition, Applicants contend that *Hashimoto* and *Kimura*, taken either alone or in combination, fail to disclose, teach or suggest a droplet discharging method including at least the feature of forming selectively a lyophilic region by irradiating selectively the object to be treated in which the liquid-repellent region is formed with light by the light irradiation unit in the second treatment chamber so that the object to be

treated includes the lyophilic region and the liquid-repellent region, as recited in present independent claim 32.

With regard to independent claim 18, as seen on pages 2-3 of the Office Action, the Examiner purports (emphasis added) that *Hashimoto* discloses "forming a first liquid-repellent region by a plasma treatment on a surface for forming a gate electrode in an upper portion of the semiconductor film ([0087] and [0097-0098]); forming selectively a first lyophilic region in the first liquid-repellent region; and forming conductive film in the first lyophilic region of the surface of the semiconductor film dropping a composition including a conductive material ([0121])." However, in a contradictory statement, the Examiner also states, on page 4 of the Office Action, that *Hashimoto* "fails to show, pertaining to claim 18, forming selectively a (first) lyophilic region in the liquid-repellent region so that the surface includes the lyophilic region and the liquid-repellent region."

In the presently claimed invention, a method for manufacturing a thin film transistor which includes selectively forming a lyophilic region in the liquid-repellent region and forming a wiring or the like by a droplet discharging method so that the width of the wiring or the like can be narrower.

Hashimoto appears to disclose that a step of forming patterns of the lyophilic portion and the liquid-repellent portion by using a mask, and a step of providing alignment marks for precisely applying a coating on the lyophilic pattern are required to selectively form a lyophilic region complicate the process for forming a film pattern (see *Hashimoto*, e.g., paragraph [0027] and [0028]). *Hashimoto* also appears to disclose that it becomes difficult to increase the film thickness due to the discharge being performed onto the lyophilic portion, then the droplets spread by wetting, in the case where a film pattern is formed on the lyophilic portion on a substrate, on which patterns of a liquid-repellent portion and the lyophilic portion were formed beforehand by an ink-jet method (see *Hashimoto*, e.g., paragraphs [0026]-[0028]). One object of the disclosure of *Hashimoto* is to provide a method for forming a film pattern, in which an increase in film thickness is achieved efficiently with simple steps (see *Hashimoto*, e.g., paragraph [0029]). Consequently, *Hashimoto* does not require forming selectively a lyophilic region in the liquid-repellent region because this would complicate the method of *Hashimoto* and it would be difficult to increase the film thickness. In other words, *Hashimoto* teaches away

from the claimed invention.

Moreover, while present independent claim 18 is directed to a method for manufacturing a thin film transistor, *Hashimoto* on the other hand is directed to (emphasis added) an "APPARATUS AND METHOD FOR FORMING FILM PATTERN" (see *Hashimoto*, e.g., the Title), which is different from the claimed invention.

Additionally, *Kimura* appears to disclose the irradiation of a specific region in a surface to be treated with laser light, laser irradiation in *Kimura* is used to form an irradiated region which is a region for forming TFT for a driving circuit with fast switching characteristics, and a non-irradiated region which is a region for forming a TFT for a pixel with a withstand high voltage (see *Kimura*, e.g., paragraph [0038]). That is, *Kimura* does not selectively form wiring or the like on the irradiated region, therefore the teachings of *Kimura* are unrelated to those of *Hashimoto*.

Furthermore, *Hashimoto* does not teach forming a thin film transistor, and there is no need for *Hashimoto* to irradiate the surface to be treated with laser light in order to obtain fast switching characteristics, as disclosed in *Kimura*. Therefore, one of ordinary skill in the art of the formation of thin film transistors, at the time that the present invention was made, would not have looked to the disclosure of *Kimura* to remedy the deficiencies of *Hashimoto* thereby arriving at the method of forming a thin film transistor, as in present independent claim 18.

Turning now to present independent claims 31 and 32, the Examiner asserts in the "Response to Arguments" section, on page 10 of the Office Action, that "Hashimoto teaches forming conductive films on the treated surface using conventional ink-jet processing that includes a droplet discharging unit and a light irradiation unit (figure 7; [0102], [0145-0148])."

However, *Hashimoto* appears to teach that the heater 15 in FIG. 7 can be a device for heat-treating the substrate by lamp annealing, which performs vaporization and drying of the discharged liquid onto the substrate, and additionally, which performs a heat treatment for the conversion into the conductive film (see *Hashimoto*, e.g., paragraph [0154]). That is, *Hashimoto* irradiates discharged liquid onto the substrate with the lamp after discharging the droplet. In the present invention, however, irradiation to selectively form the lyophilic region in the liquid-

repellent region with laser light performed before discharging the droplet.

Therefore, *Hashimoto* does not teach selectively forming a lyophilic region by selectively irradiating the object to be treated in which the liquid-repellent region is formed with light by the light irradiation unit, or selectively forming a lyophilic region in a liquid-repellent region, as argued above with respect to independent claim 18. *Kimura* fails to remedy these deficiencies with respect to present independent claims 31 and 32.

Therefore, for at least the reasons set forth above, Applicants contend that neither *Hashimoto* nor *Kimura*, taken either alone or in combination, anticipate or render obvious each and every feature recited in independent claims 18, 31, and 32. Consequently, the Examiner has failed to set forth a proper *prima facie* case of obviousness in the rejection of these claims. Applicants request the withdrawal of the rejection, and the allowance of independent claims 18, 31, and 32.

Claims 23, 24, 33-35, and 38 are allowable at least by virtue of their dependency from one of the independent claims, but also because they are distinguishable over the prior art. Accordingly, Applicants request reconsideration and allowance of these claims.

New claims 48 and 49 are distinguishable over the prior art, and thus are in condition for immediate allowance.

In view of the foregoing, it is submitted that the present application is in condition for allowance and a notice to that effect is respectfully requested. If, however, the Examiner deems that any issue remains after considering this response, the Examiner is invited to contact the undersigned attorney/agent to expedite the prosecution and engage in a joint effort to work out a mutually satisfactory solution.

Except for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account No. 19-2380. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

NIXON PEABODY, LLP

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/Anthony J. Canning, Reg. #62,107/
Anthony J. Canning
Registration No. 62,107

NIXON PEABODY LLP
Customer No.: 22204